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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,573	02/09/2001	Richard Schweder	PLI-806	6823

7590 03/10/2004

EXAMINER
MICHALSKI, JUSTIN I

Albert O. Cota
5460 White Oak Ave., A-331
Encino, CA 91316

ART UNIT	PAPER NUMBER
2644	2

DATE MAILED: 03/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/779,573	SCHWEDER ET AL.	
	Examiner	Art Unit	
	Justin Michalski	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 12, 15-17 and 19 are objected to because they include reference characters which are not enclosed within parentheses.

Reference characters corresponding to elements recited in the detailed description of the drawings and used in conjunction with the recitation of the same element or group of elements in the claims should be enclosed within parentheses so as to avoid confusion with other numbers or characters which may appear in the claims. See MPEP § 608.01(m).

2. Claim 15 is objected to because of the following informalities: Claim 15 refers to reference C12 which does not appear in Figure 2B with respect to the DC to AC inverter circuit. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4-10, and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bank et al. (Hereinafter "Bank") (US Patent 6,628,791) in view of Turner et al. (Hereinafter "Turner") (US Patent 3,992,585). Bank discloses a power

supply assembly (Figure 2) designed to produce a bias voltage that charges a diaphragm located on an electrolytic or electrostatic speaker (30) driven by an audio amplifier, said assembly comprising: means for converting an input audio signal from the audio amplifier to a direct current (Rectification means 13); means for receiving the direct current and producing a regulated direct-current voltage (limiter 40); and means for limiting a direct current high voltage prior to being applied as the output bias voltage to the diaphragm (limiter 40). Bank does not disclose converting the direct-current voltage to a high voltage alternating current and then to a high voltage direct current. Vosteen discloses a high voltage amplifier which converts a low voltage signal (Figure 1, output of amplifier 10) into a high voltage alternating current signal (Inverter step-up transformers T1 and T2) (Column 2, lines 65-68) and then converts the signals into a high voltage direct current signal (rectifier filters 21, and 22) (Column 3, lines 1-6). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the methods of Bank and Vosteen to create a high voltage gain with reduced power supply voltage (Vosteen Column 1, lines 25-31).

Regarding Claim 2, Bank further discloses converting an audio signal to a dc signal using a rectifier (Column 4, lines 28-31)

Regarding Claim 4, Bank further discloses (Figure 6) regulator (42a) whose desired (i.e. adjustable) voltage is determined by the number of diodes (Column 5, lines 21-28)

Regarding Claim 5, Bank as modified discloses a regulator as stated above apropos of claim 4. It would have been obvious to one of ordinary skill in the art at the

time the invention was made to use a commercially available regulator such as a National Semiconductor LM117T to regulate a signal and to simplify the power supply design.

Regarding Claim 6, Vosteen further discloses the dc to ac converter being an inverter (Column 2, line 65).

Regarding Claim 7, Bank as modified discloses a dc to ac inverter as stated apropos of claim 7. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a commercially available inverter such as a JKL BXA-501 as a matter of design choice to simplify the power supply design.

Regarding Claim 8, Vosteen further discloses converting the high voltage ac to dc comprises a rectifier circuit (21 and 22) which may be used in conjunction with a voltage multiplier to provide further multiplication (i.e. eight time) (Column 3, lines 1-6).

Regarding Claim 9, Vosteen further discloses multiplication of a signal if desired (i.e. adjustable output from 1.25kV to 5.6kV) (Column 3, lines 1-6).

5. Regarding Claim 10, Bank discloses a power supply assembly (Figure 2) designed to produce a bias voltage that charges a diaphragm located on an electrolytic or electrostatic speaker (30) driven by an audio amplifier, said assembly comprising: a rectifier and filter circuit (13) having means for receiving from the audio amplifier an input audio signal that is rectified and filtered to produce a direct current; a adjustable regulator circuit (limiter 40) having means for receiving the direct current and producing a regulated direct current voltage that is set to an optimum level; and a current limiter circuit (limiter 40) having means for receiving and limiting a voltage dc signal prior to

being applied as the output bias voltage to the diaphragm. Bank does not disclose converting the direct-current voltage to a high voltage alternating current and then to a high voltage direct current. Vosteen discloses a high voltage amplifier which converts a low voltage signal (Figure 1, output of amplifier 10) into a high voltage alternating current signal (Inverter step-up transformers T1 and T2) (Column 2, lines 65-68) and then converts the signals into a high voltage direct current signal (rectifier filters 21, and 22) (Column 3, lines 1-6). Vosteen further discloses converting the high voltage ac to dc comprises a rectifier circuit (21 and 22) which may be used in conjunction with a voltage multiplier to provide further multiplication (i.e. eight time) (Column 3, lines 1-6). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the methods of Bank and Vosteen to create a high voltage gain with reduced power supply voltage (Vosteen Column 1, lines 25-31).

Regarding Claims 15, Bank as modified discloses an assembly as stated above apropos of claim 14 but does not disclose the inverter being an integrated circuit. However, it is known in the art that circuits can be fabricated using integrated circuit technology in order to save space and simplify assembly of an electronic device.

Regarding Claims 16, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a commercially available inverter circuit such as a JKL Components Inc. BXA-501 to simplify the power supply design.

Regarding Claim 17, Bank further discloses a rectifier circuit (Figure 6, circuit 13) comprising capacitors 15a and 15b and diodes 13c and 13d. Although Bank does not disclose the rectifier being an integrated circuit, it is known in the art that circuits can be

fabricated using integrated circuit technology in order to save space and simplify assembly of an electronic device.

Regarding Claim 18, Bank further discloses resistor ladder (Figure 6, resistors 17a and 17b).

Regarding Claim 19, Bank further discloses the resistor ladder network (Figure 6) resistor 17b where the bias voltage is produced and a capacitor (41) connected to ground (50) (i.e. virtual ground).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bank as modified in view of Turner et al. (Hereinafter "Turner") (US Patent 3,992,585). Although Bank as modified does not explicitly disclose the rectifier being a full wave rectifier it is known in the art that a full wave rectifier can be used to convert an ac signal into a dc signal as illustrated in Turner (diodes 23, 24, and 25) (Column 3, lines 11-12).

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bank as modified as applied to claim 10, in further view of Turner et al. (US Patent 3,992,585).

Regarding Claim 11, although Bank as modified does not explicitly disclose the rectifier being a full wave rectifier it is known in the art that a full wave rectifier can be used to convert an ac signal into a dc signal as illustrated in Turner (diodes 23, 24, and 25) (Column 3, lines 11-12).

8. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bank as modified as applied to claim 10, in further view of Quick (US Patent 4,447,783).

Regarding Claim 12, Bank as modified discloses an assembly as stated apropos of claim 11 but does not disclose the regulator being an integrated circuit or the use of potentiometers. However, it is known in the art that circuits can be fabricated using integrated circuit technology in order to save space and simplify assembly of an electronic device. It is also known that potentiometers can be used to make adjustments to parameters of a circuit including bias voltages as disclosed by Quick (Column 5, lines 1-4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include an integrated circuit and potentiometers to decrease the size an be able to change the bias voltage to a desired level.

Regarding Claim 13, Bank as modified discloses a regulator as stated above apropos of claim 12. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a commercially available regulator such as a National Semiconductor LM117T to regulate a signal and to simplify the power supply design.

Regarding Claim 14, Bank further discloses the bias voltage on diode 13e can exceed 3000 volts (i.e. between 3000 and 500 volts) (Column 5, line 62).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin Michalski whose telephone number is (703)305-5598. The examiner can normally be reached on 8 Hours, 5 day/week.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Isen can be reached on (703)305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JIM

XU MEI
PRIMARY EXAMINER